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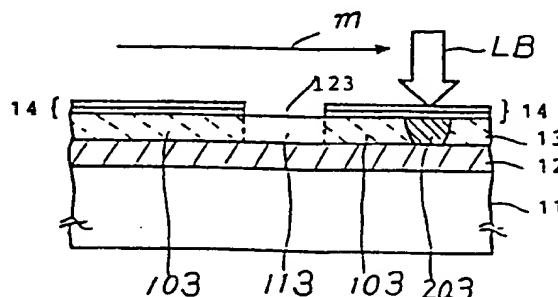
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(54) A manufacturing method of an integrated circuit based on the semiconductor-on-insulator technology and a device so manufactured.

(57) Random layout of devices or active regions of the devices is allowed for a semiconductor integrated circuit based on an SOI technology using an anti-reflecting film (14). Openings (123) are provided for the anti-reflecting film (14) formed on a polycrystalline silicon layer (13), corresponding to the device regions wherein devices or active regions of the devices are to be formed. An overlapped scan of a laser (LB) beam having diameter larger than the dimension of the openings (123) is applied on the silicon layer (13) through the openings (123) and circumferential anti-reflecting film (14). Concave temperature profile is achieved along every directions (m) across the openings due to the enhanced beam (LB) absorption by the circumferential anti-reflecting film (14), hence recrystallization nucleation of the silicon layer initiates at the center of each opening during the laser beam scan. Thus, self-aligned single crystal regions (113) are fabricated in the polycrystalline silicon layer (13) at the respective predetermined device regions. The channel region of an IG-FET is exclusively formed in the single crystal region (113) and the source or drain regions are formed in adjacent polysilicon regions.

*FIG. 4(c)*



TITLE OF THE INVENTION

A Fabrication Method of a Semiconductor Integrated Circuit  
and a Device Fabricated by Using the Same

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device based on so-called SOI (semiconductor on insulator) technology, particularly to a method for fabricating the semiconductor device by using an anti-reflecting film for laser beam irradiation.

SOI technology has been receiving increasing interests because of its attractive capabilities of providing integrated circuits (ICs) with increased breakdown voltages between isolated circuit components such as transistors and so forth, and also with improved operating speeds due to reduced parasitic capacitances between the circuit components and a substrate the circuit components formed thereon. The outstanding feature of SOI technology is the capability of providing three-dimensional ICs considered as the most promising means of breakthrough for the limitation to the integration density in conventional ICs.

In the early stage of SOI technology, efforts were directed to obtaining a recrystallized region as large as possible in a polycrystalline semiconductor layer such as a polysilicon layer. This resulted in the difficulty of forming a grain boundary free region at desired position in the semiconductor layer. If a grain boundary locates in

1 the active region of a transistor, for example, formed in  
the recrystallized region, characteristics of the  
5 transistor cannot be comparable to ordinary transistors  
fabricated on single crystal silicon substrates. Such  
grain boundary becomes the causes of increased leakage  
currents and nonuniformity of threshold voltages of the  
10 transistors.

Recent development in the SOI technology rather seems  
to be concentrated to selective recrystallization of an  
amorphous or polycrystalline semiconductor layer. That is,  
15 only predetermined regions of a semiconductor layer, in  
each of which an active component such as transistor is to  
be formed, are recrystallized into single crystal islands.  
Though originally proposed for increasing efficiency of the  
20 light beam irradiation for recrystallizing a semiconductor  
layer, anti-reflecting film coating has been reported to be  
advantageous for such selective recrystallization if it is  
modified into a stripe structure. (Colinge et al; Applied  
25 Physics Letters, vol.41, p.346, 1982). In this method,  
transversely arranged stripes of anti-reflecting film are  
formed on a amorphous or polycrystalline silicon layer. A  
30 laser beam having diameter large enough to cover at least  
two adjacent stripes is scanned along the center line  
between the stripes. The laser beam energy is controlled  
to be at slightly above the lowest level necessary for  
35 melting the uncoated region of the silicon layer. Thus, a  
desired concaved temperature profile in the lateral

1 direction can be achieved thanks to the greater beam  
absorption by the stripes of anti-reflecting film. This  
method will be described in some detail in the following.

5 FIGs.1(a) and 1(b) are schematic illustrations of an  
amorphous or polycrystalline silicon layer and  
stripe-structured anti-reflecting films successively formed  
on an amorphous insulating layer, wherein FIG.1(a) is a  
10 plan view and FIG.1(b) is a cross-section taken along the  
line B-B in FIG.1(a).

Referring to FIG.1(a) and 1(b), an amorphous or  
15 polycrystalline silicon layer 22, which is to be  
recrystallized into a single crystal, is deposited on an  
amorphous insulating layer 21. An anti-reflecting film 23  
of silicon nitride,  $\text{Si}_3\text{N}_4$ , is formed on the silicon layer  
20 22, and then, delineated into stripe structures 23 as shown  
in FIGs.1(a) and 1(b). If thickness of the anti-reflecting  
film stripes 23 is adequately controlled, the reflectivity  
of the surface of the silicon layer 22 at the region coated  
25 with the stripe 23 can approximately be 5% in contrast to  
that of 60% at the uncoated region. As a result, when a  
irradiation or laser beam, an argon ion laser beam, for  
example, having a spot diameter larger than the distance  
30 between the stripes 23 is applied, temperature distribution  
profile as shown in FIG.1(c) is obtained in the lateral  
direction (i.e. the direction along B-B line in FIG.1(a)).  
35 In FIG.1(c), ordinate indicates temperature T and abscissa  
indicates the position between the stripes 23. As shown in

1 FIG.1(c), the temperature T is lowest at the center of the  
stripes 23.

5 When a laser beam is scanned along the center line  
between the stripes 23 in the direction as indicated by the  
arrow in FIG.1(a), recrystallization front edges in the  
silicon layer is schematically indicated by a curve 25  
0 which moves upward according to the scanning of the laser  
beam. In FIG.1(a), two curves 25 correspond to respective  
recrystallization fronts at two different moments. Each of  
the curves 25 indicates a solid-liquid interface and  
5 melting point of the silicon layer 22 distributes along the  
curve 25. Because the curve 25 (solid-liquid interface  
line) has curvature bending behind the front edge, the  
growth of a crystal grain nucleated from a virtual seed on  
10 the center line is dominant, and finally, spreads over the  
region between the stripes 23. As a result, grain  
boundaries between the above mentioned dominant grain and  
other subdominant grains are going to be swept from the  
15 region between the stripes 23 and accumulate under the  
stripes 23. Similar concaved temperature profile is  
obtained by using a doughnut-shaped laser beam and  
20 successful recrystallization is achieved in a polysilicon  
layer on an amorphous layer. (Kawamura et al; Applied  
Physics Letters, vol.40, p.394, 1982)

25 Thus, with the use of anti-reflecting film stripes, it  
is reported that a single crystallized region of 20x100  
square microns can be formed in a silicon layer on an

1 amorphous insulating layer. The stripe-structured  
anti-reflecting film permits laser beam to be efficient and  
5 simple of its shape as a round beam. However, the  
stripe-structured anti-reflecting film methodology  
inevitably decreases the freedom in the device pattern  
layout on a semiconductor layer.

10 Referring to FIGs.1(a) and 1(b), if devices such as  
transistors or at least active regions of the devices are  
respectively located in regions 26a and 26b of the  
semiconductor layer 22, one of the devices or active  
15 regions of the devices can be formed in a  
single-crystallized region 26a, but another formed in a  
region 26b can not be free of a grain boundary because of  
the reason as described before. Since grain boundaries  
20 provide the device with the aforesaid undesirable  
influences, the device pattern layout can not but be  
restricted within the region between the anti-reflecting  
film stripes 23. This means that random layout of the  
25 devices or active regions of the devices is substantially  
inhibited and the devices or the active regions must be  
positioned in a relatively orderly arrangement instead.  
30 As a result, SOI technology using anti-reflecting film  
stripes is suitable to integrated circuits (ICs) such as  
those based on gate array methodology but is rather not  
suitable to ICs requiring random arrangement of devices as  
35 in logic ICs. Thus, the anti-reflecting film stripe



1 methodology also restricts efficient use of semiconductor  
area in ICs based on SOI.

5 SUMMARY OF THE INVENTION

It is an object of the present invention to provide a  
semiconductor integrated circuit based on an SOI technology  
10 using an anti-reflecting film, wherein the layout of  
devices on a semiconductor layer can be substantially  
random.

It is another object of the present invention to  
15 provide a semiconductor integrated circuit based on an SOI  
technology using an anti-reflecting film, wherein effective  
use of semiconductor area can be achieved.

It is further another object of the present invention  
20 to provide an insulated-gate transistor based on an SOI  
technology with improved fabrication yield.

The above objects can be attained by fabricating a  
semiconductor integrated circuit based on an SOI technology  
25 using an anti-reflecting layer but not in the form of  
stripes. The fabrication method comprising steps of: (a)  
forming an amorphous or polycrystalline semiconductor layer  
on an amorphous insulating layer; (b) forming an  
30 anti-reflecting film to a light beam on the semiconductor  
layer; (c) selectively forming openings at respective  
predetermined portions of the anti-reflecting film; (d)  
35 irradiating the light beam to an area of surface of the  
anti-reflecting film, thereby including at least one of

the openings, on conditions that the semiconductor layer is recrystallized to be free of grain boundaries at the opening; and (e) forming a semiconductor device or active region of the device in the recrystallized semiconductor layer at the opening. In accordance with the method, the channel region of an insulated-gate field effect transistor (IG-FET) or metal oxide semiconductor (MOS) transistor is exclusively formed in a recrystallized semiconductor layer at the opening.

#### BRIEF DESCRIPTION OF DRAWINGS

The above and other objects and advantages of the present invention will become apparent from the following description of embodiments with reference to accompanying drawings forming a part thereof, wherein:

FIGs.1(a) and 1(b) are schematic illustrations of an amorphous or polycrystalline silicon layer formed on an amorphous insulating layer and stripes of anti-reflecting layer formed on the silicon layer, wherein FIG.1(a) is a plan view and FIG.1(b) is a cross-section taken along the line B-B in FIG.1(a);

FIG.1(c) is a temperature distribution profile obtained in the direction along B-B line in FIG.1(a);

FIGs.2(a) and 2(b) are a plan view and enlarged cross-section taken along line B-B in FIG.2(a) in accordance with an embodiment of the present invention.

1           FIG.3(a) is a plan view schematically illustrating the  
growth of single recrystallized region at an opening  
5           according to the present invention;

FIGs.3(b) and 3(c) are respective temperature  
distribution profiles on the lines E-E and F-F in FIG.3(a);

10           FIGs.4(a) to 4(g) are cross-sections at the respective  
fabrication steps of a semiconductor device based on an SOI  
technology; and

15           FIGs.5(a) to 5(d) show yet another embodiment of the  
present invention.

#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

20           An embodiment of the present invention is shown in a  
plan view of FIG.2(a) and an enlarged cross-section of  
FIG.2(b) taken along line B-B in FIG.2(b). Referring first  
to FIG.2(b), as a substrate, an insulating layer of  $\text{SiO}_2$   
layer 4 of thickness of about 1 micron is formed on a  
25           silicon wafer 3 by using a thermal oxidation process, for  
example. Respective one of silicon nitride layer 5 and  
polysilicon layer 6 having thicknesses of 1000 Å and 4000  
Å, respectively, are successively formed on the  $\text{SiO}_2$  layer  
30           4 by using low pressure chemical vapor deposition (LPCVD)  
methods, for example. The polysilicon layer 6 is the layer  
to be subject to a recrystallization process later, and the  
silicon nitride layer 5 is for improving adhesion of the  
35           polysilicon layer 6 to the  $\text{SiO}_2$  layer 4 after the  
recrystallization. A  $\text{SiO}_2$  layer 7 of about 300 Å is formed

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by thermally oxidizing the surface of the polysilicon layer 6 and then a silicon nitride layer 8 of about 300 Å is deposited thereon by using an LPCVD method, for example. The SiO<sub>2</sub> layer 7 and silicon nitride layer 8 constitute anti-reflecting film 2 in FIG.2(a). The thickness of the anti-reflecting film 2 is determined according to the wave length of laser beam for the recrystallization and the refractive index of the layer materials to the wave length. The anti-reflecting film may comprises a single layer of either of SiO<sub>2</sub> or silicon nitride, however, the double-layered structure of the anti-reflecting film allows to take advantages as described in later.

Referring back to FIG.2(a), the anti-reflecting layer 2 is provided with substantially rectangular-shaped openings (windows) 1a, 1b, 1c and so forth, instead of being formed into the stripe structure in the prior art as shown in FIGs.1(a) and 1(b). Each of the openings is positioned so as to correspond to a device region (the region in which a device such as transistor or the active region such as channel region of the transistor is formed). The dimension of the opening is 10 to 20 microns, for example.

A light beam from a cw (continuous wave) Ar ion laser, for example, having output power of 8 to 14 watts is scanned over the anti-reflecting film 2 and the polysilicon layer at the openings 1a, 1b, 1c and so forth at a speed of 5 cm/sec. The scan of the laser beam is carried out by

1 translating the wafer 3 relative to a fixed beam or it may  
be done vice versa, wherein scanning pitch is controlled to  
5 be smaller than the diameter of the beam D so that the  
traces of the scanned beam overlap each other. A  
preferable overlap ratio is approximately 70 per cent of  
the beam diameter. The beam diameter D is 80 to 100  
0 microns in terms of the width of irradiated region on the  
substrate. The dimension of an opening is 10 to 20 microns  
as mentioned before. Hence, since the beam is relatively  
larger than the openings (4 to 10 times) and the scanning  
5 speed is relatively high compared with the dimension of  
openings, the polysilicon layer at each opening can be  
assumed to be heated with a pulse of a fixed beam. In the  
above, the beam for the recrystallization should not be  
0 limited to a laser beam but other energy beam such as a  
focused emission of a mercury lamp may be employed if it  
can provide a sufficient energy density.

5 FIG.3(a) is a plan view schematically illustrating the  
growth of single recrystallized region in an opening, for  
example, the opening 1a in FIG.2(a). FIGs.3(b) and 3(c)  
are temperature distribution profiles along the lines E-E  
and F-F in FIG.3(a), respectively, wherein T indicates  
0 temperature and coordinates on the respective axes  
perpendicular to the temperature axes indicate the position  
on lines E-E and F-F. The same as in the prior art using  
15 stripe-structured anti-reflecting film as described with  
reference to FIGs.1(a) to 1(c), the temperature T is lowest

1 at the center of the opening 1a in both E-E and F-F  
directions and increases toward the periphery of the  
5 opening 1a because of the greater absorption of the laser  
beam irradiation by the anti-reflecting film 2. As a  
result, recrystallization of the polysilicon layer  
initiates from the nucleus 9 at the center of the opening  
1 immediately after the cease of the pulsed laser beam  
irradiation. A substantially isotropic recrystallization  
occurs to spread as shown by circles 10 in FIG.1(a), and  
finally, fills in the opening 1a. Thus, a  
grain-boundary-free single crystal polysilicon layer is  
formed in the opening 1a, and similarly in other openings.

Another embodiment of the present invention will be  
described in the following with reference to FIGs.4(a) to  
4(g) illustrating cross-sections at the respective  
fabrication steps of a semiconductor device based on SOI  
technology.

Referring to FIG.4(a), a  $\text{SiO}_2$  insulating layer 12 of  
thickness of about 1 micron is formed on a silicon  
substrate 11 by using a thermal oxidation process, and  
then, an amorphous or polycrystalline silicon layer 13 of  
thickness of about 4000 Å is deposited on the insulating  
layer 12 by using a CVD (chemical vapor deposition) method.  
In the following description of this embodiment, a  
polysilicon layer stands for the silicon layer 13. The  
polysilicon layer 13 is then doped with a predetermined  
concentration of boron, B, as a p-type impurity by an ion

1 implantation technique. Thus, the polysilicon layer 13 is  
provided with p-type conductivity.

5 A  $\text{SiO}_2$  thin film 121 of thickness of about 300 Å is  
formed on the polysilicon layer 13 by using a thermal  
oxidation process, and then a silicon nitride ( $\text{Si}_3\text{N}_4$ ) film  
122 of thickness of about 300 Å is deposited on the  $\text{SiO}_2$   
10 film 121 by a CVD method. The  $\text{SiO}_2$  film 121 and  $\text{Si}_3\text{N}_4$  film  
122 are selectively removed as shown in FIG.4(b) by using a  
conventional photolithographic technique so that openings  
throughout the films are formed at predetermined regions  
15 Ach. Each of the regions is referred to as device region  
in which an insulated gate field effect transistor (IG-FET)  
or at least the channel of the transistor is to be formed.  
In FIG.4(b), only one opening 123 is illustrated.

20 The  $\text{SiO}_2$  film 121 and  $\text{Si}_3\text{N}_4$  film 122 constitutes an  
anti-reflecting film to the laser beam irradiation. The  
anti-reflecting film may comprise either one of  $\text{SiO}_2$  or  
25  $\text{Si}_3\text{N}_4$  film as mentioned before, however, the double-layered  
anti-reflecting film as shown in FIG.4(b) permit to take  
advantage of large etching rate difference between  $\text{SiO}_2$  and  
 $\text{Si}_3\text{N}_4$  or silicon to etchants such as carbon tetra-fluoride  
30 ( $\text{CF}_4$ ) gas and a hydrochloric acid (HF) solution. For  
instance, during a dry etching process for forming the  
opening 123, the  $\text{SiO}_2$  film 121 having a relatively low  
etching rate compared with those of the  $\text{Si}_3\text{N}_4$  film 122 and  
35 polysilicon layer 13 plays a role of a stopping layer  
against the etching by an etchant gas such as  $\text{CF}_4$  but it

1 can easily be removed by HF solution without affecting the  
polysilicon layer 13. Thus, the process for forming  
5 precision openings 123 in the anti-reflecting film on the  
polysilicon layer 123 can be facilitated.

During the substrate 11 is heated at about 450°C in  
atmospheric air, scan of a laser beam LB, Ar ion laser, for  
example, in the direction of an arrow m is applied to the  
polysilicon layer 13 through the anti-reflecting film 14 as  
shown in FIG.4(c). Hence, every portions of the  
polysilicon layer 13 are brought into a molten state once  
according to the scan of the laser beam, and its  
corresponding region to the opening 123 is recrystallized  
into a single crystal 113. In FIG.4(c), references 103 and  
203 designate a domain recrystallized into a  
polycrystalline state and that in molten state,  
respectively.

Intensity and scanning speed of the laser beam LB are  
controlled to be enough for melting the polysilicon layer  
13 under the anti-reflecting film 14 which decreases the  
reflectivity of the surface of the polysilicon layer 13 to  
about 5 per cent but insufficient for melting a polysilicon  
layer alone having surface reflectivity of about 60 per  
cent alone. (i.e. the laser beam is too weak to raise the  
polysilicon layer 13 at the opening 123 up to the melting  
point if no anti-reflecting layer 14 is formed around the  
opening 123.) Exemplary conditions complying with such  
requirement are as follows:



1

Laser output: 10 Watts

Laser beam diameter: 50 microns

5

Scanning speed: 5 cm/sec

10

In the above, the laser beam diameter is defined in terms of the width of melted region of a polycrystalline layer coated with an anti-reflecting film when a laser beam is scanned thereon.

15

With the scan of a laser beam under the above conditions, recrystallization of the polysilicon layer 13 initiates at the center of the opening 123 and spreads therein as explained with reference to FIG.3 (a). Thus, the polysilicon layer 13 at the opening 123 becomes single crystal, however, desirable recrystallization into a single crystal layer does not occur in the circumferential polysilicon layer 13 under the anti-reflecting film 14 as mentioned before.

20

25

In accordance with the object of the present invention, a number of openings in an anti-reflecting film can be positioned randomly, corresponding to the regions, each for forming a device or active region of the device therein. As a result, it is probable that when a laser beam is scanned with aforesaid overlapping manner, the edge of the laser beam occasionally crosses over an opening at which the polysilicon layer has already been single-crystallized. However, the single-crystallized layer in the region would not be melted again by the laser beam scan, because heat necessary for the

30

35

1 single-crystallized region to reach again its melting point  
is not supplied from the un-irradiated side region of the  
opening.

5 After the polysilicon layer 13 at each opening 123 is  
recrystallized to be grain boundary free (whereas each  
corresponding circumferential region is recrystallized as a  
polycrystal layer), the  $\text{Si}_3\text{N}_4$  film 122 and  $\text{SiO}_2$  film 121  
constituting the anti-reflecting film 14 are removed by  
using a hot phosphoric acid solution and a hydrofluoric  
acid solution, respectively. Then, the polysilicon layer  
13 is formed into islands so that each island includes one  
of the single-crystallized region 113 and corresponding  
polycrystalline circumferential region 103, as shown in  
FIG.4(d).

0 The surface of the island is thermally oxidized, hence  
a gate oxide layer 15 having a predetermined thickness is  
formed as shown in FIG.4(e). Subsequently, a polysilicon  
layer of thickness of about 4000 Å is formed on the island  
by a conventional CVD process and selectively etched by  
using an ordinary photolithographic technique so that a  
gate electrode 16 is left on the single-crystallized region  
113.

5 Following the above, high concentration of an impurity  
such as arsenic (As) is ion-implanted into the silicon  
layer 103 with the use of polysilicon gate electrode 16 as  
a mask, hence  $n^+$ -type source or drain regions 17 and 18 are  
formed after an annealing at temperature 1050°C, as shown

1 in FIG.4(f). Thus, basic structure of an insulated-gate  
field effect transistor (IG-FET) or MOS transistor is  
5 completed based on SOI technology.

An insulating coating layer 19 is formed on each of  
the transistor structure. The insulating coating layer 19  
having thickness of about 8000 Å is, then, provided with  
10 contact holes 100 through which connections to the source  
or drain regions 17 and 18 are provided by the respective  
wiring layers 110 and 120 of aluminum, for example, as  
shown in FIG.(g). If a PSG (phospho-silicate glass) layer  
15 is used for the insulating coating layer 19, a heat process  
(conventionally referred to as a reflow process) at 1050°C,  
for example, is needed for blunting the sharp edge of the  
contact holes 100.

20 As described above, a heat process at a temperature as  
high as 1050°C is necessary for the annealing of the  
ion-implanted source or drain regions 17 and 18 or the  
25 reflow process for the contact holes 100 in a PSG layer.  
The heat process at such high temperature tends to cause  
diffusion of doped impurities from the source or drain  
regions 17 and 18 to the single crystal region 113. If a  
30 grain boundary should exist in the single crystal region  
113, the impurity diffusion along the grain boundary would  
be accelerated, and thus, the problems in the prior art,  
such as increased leak currents, non-uniform threshold  
35 voltages, source-drain breakdown failures, etc. in the

1 devices formed in the recrystallized semiconductor layer,  
would occur.

6 Again, in the prior art SOI technology using  
anti-reflecting film, it is substantially impossible to  
recrystallize a semiconductor layer selectively only at the  
device regions. As a result, the regions to be grain  
0 boundary free are formed inevitably large in order to  
provide some degree of freedom in the arrangement of the  
devices. This results in difficulty in the fabrication and  
poor yield of semiconductor integrated circuits based on  
5 the SOI technology. On the other hand, according to the  
present invention, it is possible to recrystallize a  
semiconductor layer at arbitrary regions corresponding to  
the device regions, as explained in the above embodiments.  
10 As a result, small semiconductor regions, each of which  
afford to accommodate at least the active region of a  
device, for example, a channel region of an IG-FET, can  
selectively be grain boundary free, corresponding to the  
25 device layout. Thus, according to the present invention,  
the IG-FETs, for example, in a semiconductor integrated  
circuit based on an SOI technology can be free from the  
prior art problems relating to the grain boundaries, and  
30 therefore, superior characteristics and greater fabrication  
yield of the integrated circuit can also be provided. It  
is obvious that entire region of a device including the  
35 source or drain regions of an IG-FET, for example, can be  
fabricated in a grain-boundary-free region formed according

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1 to the present invention, since the grain-boundary-free  
region can be large as 10x20 square microns.

5 FIGs.5(a) to 5(d) show further another embodiment of  
the present invention. A polycrystalline semiconductor  
layer 41, polysilicon layer, for example, having thickness  
of about 4000 Å is formed on an insulating layer 40 having  
10 thickness of about 1 micron, and an anti-reflecting film 42  
having an opening 421 is formed on the polysilicon layer  
41, as shown in FIG.5(a). The anti-reflecting film 42 may  
has a double-layered structure comprising a  $\text{Si}_3\text{N}_4$  layer 422  
15 and an underlying  $\text{SiO}_2$  layer 423, each having a thickness  
of about 300 Å. The polysilicon layer 41 at the opening  
421 is recrystallized to be grain boundary free by a laser  
beam irradiation, as described in the previous embodiments.  
20 The surface of the polysilicon layer 41 at the opening 421  
is thermally oxidized to form a  $\text{SiO}_2$  layer 411 of thickness  
of about 1000 Å. The anti-reflecting film 42 protects the  
polysilicon layer 41 around the opening 421 from the  
25 thermal oxidation.

The  $\text{Si}_3\text{N}_4$  layer 422 of the anti-reflecting film 42 is  
removed by using a selective etchant such hot phosphoric  
30 acid solution. The  $\text{SiO}_2$  layer 411 and the exposed  $\text{SiO}_2$   
layer 423 as shown in FIG.5(b) are subjected to a dry  
etching process using an etchant such as  $\text{CF}_4$  plasma. The  
time necessary for etching off the 300 Å  $\text{SiO}_2$  layer 423 is  
35 about 40 seconds and that for the 1000 Å  $\text{SiO}_2$  layer 411 is  
about 120 seconds. Hence, the surface of the polysilicon

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1 layer 41 around the opening 421 is first exposed to the  $\text{CF}_4$   
plasma, and subsequently etched off completely before the  
5 remaining about 700 Å  $\text{SiO}_2$  layer 411 is etched off, as  
shown in FIG.5(c), because etch rate of silicon by  $\text{CF}_4$   
plasma is about 100 times larger than that of  $\text{SiO}_2$ . The  
dry etching is continued until the  $\text{SiO}_2$  layer 411 is just  
10 removed, and finally, a single crystal island 412 of  
silicon is left on the insulating layer 40, as shown in  
FIG.5(d). Thus, self-aligned single crystal silicon  
islands can be obtained in accordance with the SOI  
15 technology of the present invention.

While the described embodiments represent the  
preferred form of the present invention, it is to be  
understood that modifications will occur to those skilled  
20 in the art without departing from the spirit of the  
invention. The scope of the present invention is therefore  
to be determined by the appended claims.

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CLAIMS

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5 1. A fabrication method of a semiconductor device,  
comprising the steps of:

forming an amorphous or polycrystalline semiconductor  
layer on an amorphous insulating layer;

10 forming an anti-reflecting film to a light beam on  
said semiconductor layer;

selectively forming openings at respective  
predetermined portions of said anti-reflecting film;

15 irradiating said light beam to an area of surface of  
said anti-reflecting film, said area including at least one  
of said openings, on conditions that said semiconductor  
layer is recrystallized to be free of grain boundaries at  
20 said opening; and

forming a semiconductor device or active region of  
said device in said recrystallized semiconductor layer at  
25 said opening.

30 2. A fabrication method of a semiconductor device as set  
forth in claim 1, wherein said semiconductor is silicon.

3. A fabrication method of a semiconductor device as set  
forth in claim 1, further comprising a step of forming an  
insulated gate electrode on said recrystallized region of  
35 said semiconductor layer, said insulated gate electrode  
comprising a gate electrode and an insulating layer formed

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between said gate electrode and said recrystallized region of said semiconductor layer.

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4. A fabrication method of a semiconductor device as set forth in claim 3, further comprising a step of forming respective regions for source and drain in said

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semiconductor layer, said source and drain regions facing each other across said recrystallized region of said semiconductor layer and abutting said recrystallized region.

15

5. A fabrication method of a semiconductor device as set forth in claim 3, wherein said semiconductor is silicon.

20

6. A fabrication method of a semiconductor device as set forth in claim 5, wherein said insulating layer is a silicon dioxide layer.

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7. A fabrication method of a semiconductor device as set forth in claim 6, wherein said silicon dioxide layer is formed by using LPCVD (low pressure chemical vapor deposition).

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8. A fabrication method of a semiconductor device as set forth in claim 6, wherein said insulating silicon dioxide layer is formed by thermally oxidizing the surface of said recrystallized region of said semiconductor layer.

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1 9. A fabrication method of a semiconductor device as set  
forth in claim 1, wherein said anti-reflecting layer  
5 comprises a silicon nitride layer.

10 10. A fabrication method of a semiconductor device as set  
forth in claim 9, wherein said anti-reflecting layer  
further comprises underlying silicon dioxide layer.

15 11. A fabrication method of a semiconductor device as set  
forth in claim 1, wherein said light beam is a laser beam.

20 12. A fabrication method of a semiconductor device as set  
forth in claim 11, wherein said laser beam is an Ar ion  
laser beam.

25 13. A fabrication method of a semiconductor device as set  
forth in claim 1, wherein said light beam is scanned over  
said anti-reflecting layer so that semiconductor regions at  
said openings are consecutively recrystallized.

30 14. An insulated-gate field-effect transistor (IG-FET)  
fabricated in a semiconductor layer formed on an amorphous  
insulating layer (24, 4, 12, 40), said semiconductor  
layer (22, 6, 13, 41) having a recrystallized region in  
which channel region of said IG-FET is exclusively  
35 formed.

FIG. 1(a)

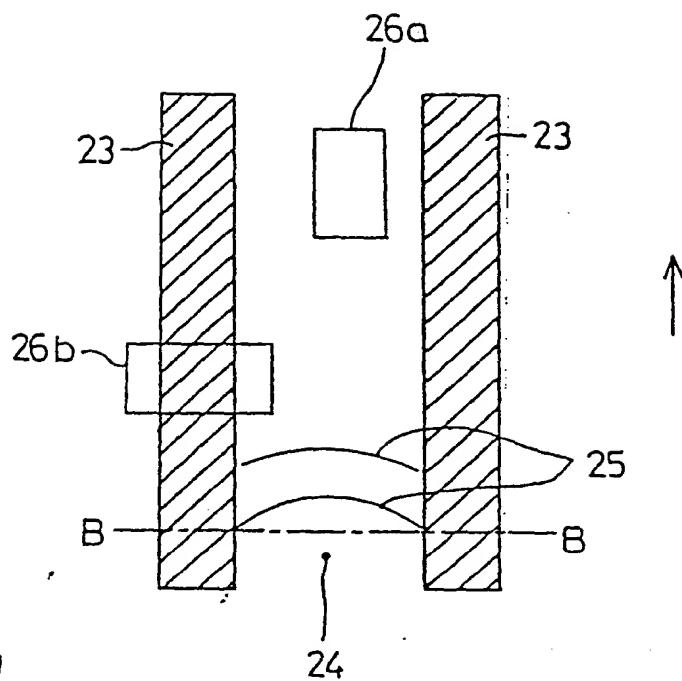


FIG. 1(b)

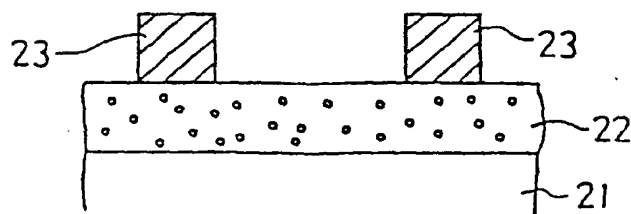


FIG. 1(c)

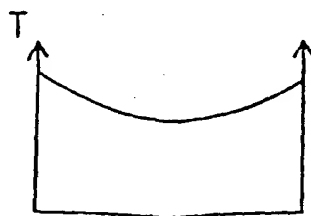


FIG. 2(a)

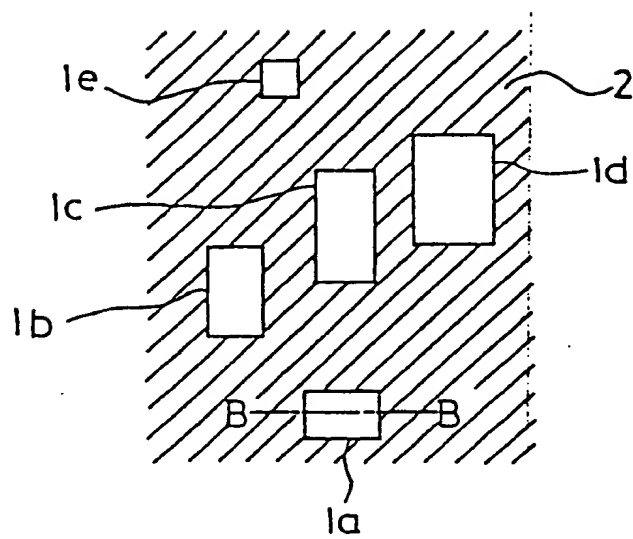


FIG. 2(b)

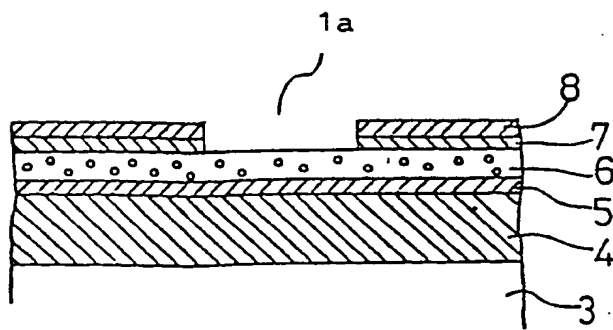


FIG. 3(a)

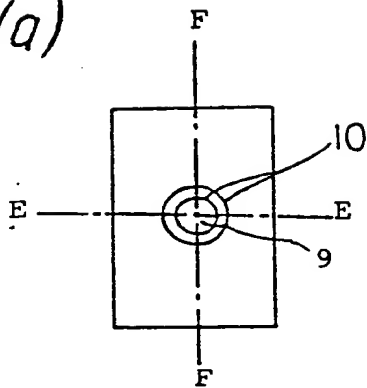


FIG. 3(c)

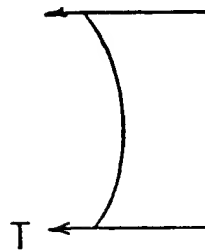


FIG. 3(b)

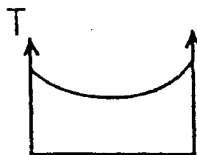


FIG. 4 (a)

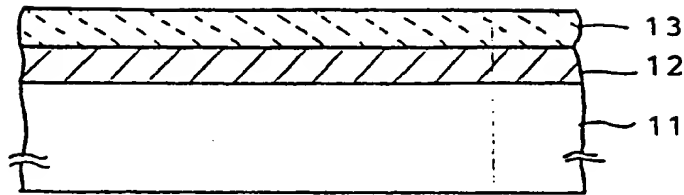


FIG. 4 (b)

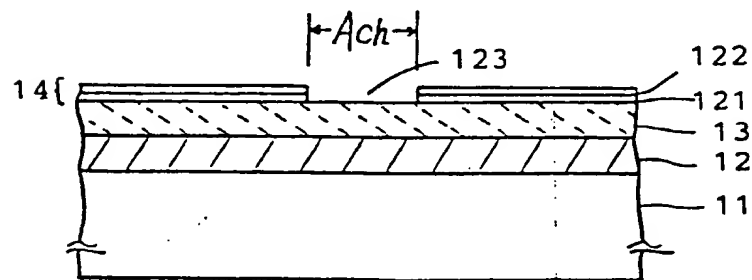


FIG. 4 (c)

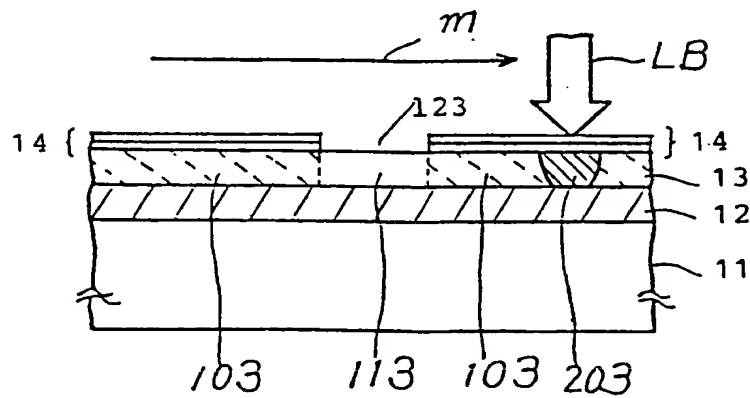


FIG. 4 (d)

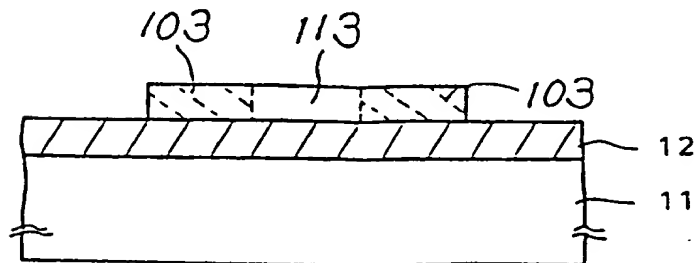


FIG. 4(e)

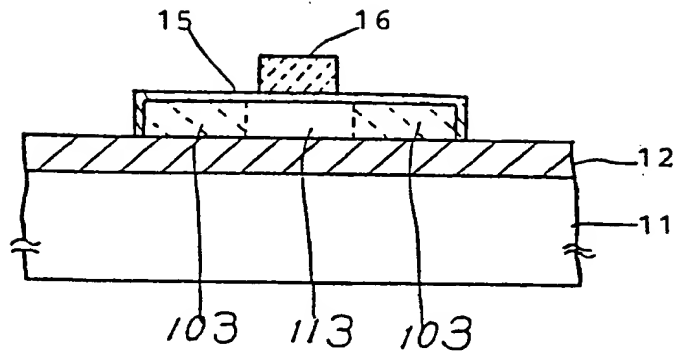


FIG. 4(f)

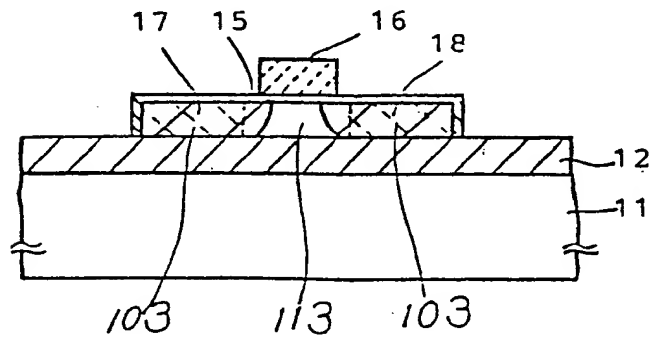


FIG. 4(g)

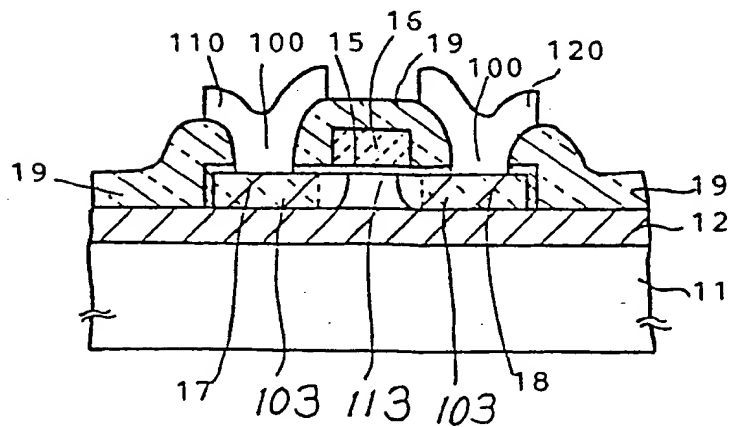


FIG. 5(a)

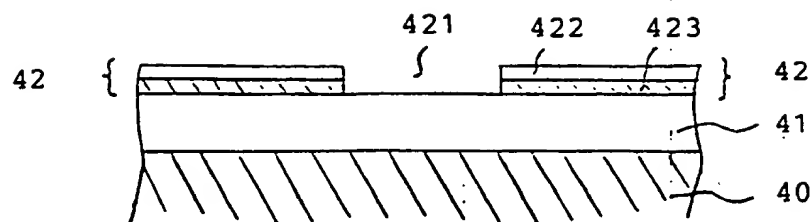


FIG. 5(b)

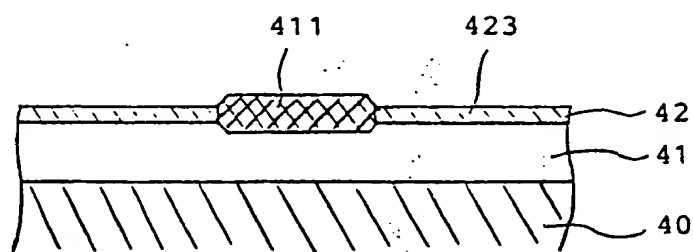


FIG. 5(c)

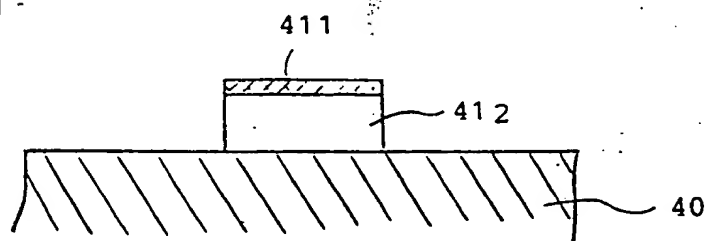
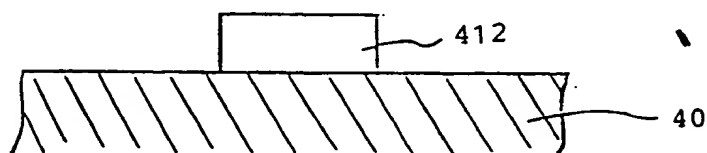


FIG. 5(d)



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